REMARKS

This paper responds to the Office Action mailed on December 28, 2005.

Claims 11, 15, 18, 22, 25, 35 and 41 are amended, no claims are canceled, and no claims are added; as a result, claims 11-25, 35-39 and 41-43 are now pending in this application.

In the Specification

The specification has been amended to update the priority data to include the patent number of parent Application No. 09/137,521. Applicant further adds an incorporation by reference statement. This is supported by the patent application transmittal filed February 16, 2001.

§112 Rejection of the Claims

Claims 11-25, 35-39 and 41-43 were rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness. Specifically, claims 11-25, 35-39 and 41-43 were rejected as prolix [MPEP 2173.05(m)], as including unnecessarily wordy and ambiguous recitations, particularly evoking wordy process limitations that do not clearly define product scope. Applicant respectfully disagrees, and submits that the wording is directed to the product as required by law.

Applicant submits that the term "polished" is definite and understood by one of ordinary skill in the art, and that the requisite degree of polishing is clear as being enough to remove the irregularities caused by sawing the die from the wafer, as noted in the specification at least at pages 2 and 8, as discussed in more detail in the previous response. However, in order to advance the prosecution of this application, Applicant has amended claims 11, 15, 18, 22, 25, 35 and 41 to remove the objected to language.

Applicant has also amended the claims to render the claims more specifically directed to the features of the final product that distinguish this application over the suggested combination of cited references. Applicant respectfully submits that the amended claims are directed to the product and not the process, and meet the requirements of the law and MPEP section 2173.05(p). In view of the above amendments, Applicant requests that this rejection be withdrawn.

§103 Rejection of the Claims

Claims 11-16, 18-25, 35-38 and 41-43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Boruta (EP 0 678 901) in view of Altavela et al. (U.S. 5,408,739) with Arlt et al. (U.S. 4,804,641). Applicant traverses this rejection.

The cited reference of Boruta discloses a method of sawing or cutting a wafer that has metal material in the scribe lines, where the metal material is wider than the saw blade (see col. 1, lines 26-30). The method includes making three saw cuts, first groove 36, spaced apart parallel second groove 38, and third groove 39 overlapping the first two cuts (see figure 2A-D and figure 3A-D; and col. 3, lines 34-50). The scribe lane has a metal test pattern (item 32 in figure 2, item 62 in figure 3, item 82 in figure 4, item 102 in figure 5) and is not an unused or blank region. Applicant respectfully submits that there is no suggestion in Boruta of having the scribe cuts made near the edge of the device circuit regions and one of ordinary skill would understand that the disclosed saw blade thickness of 1.2 to 1.6 mil (col. 2, line 58) would result in a distance to the circuit edge of about 15 to 25 microns.

The cited reference of Altavela discloses sawing the front surface of a thermal ink jet printer head so that the sawing leaves a front surface that does not require a polishing step (see Fig. 8 and col. 1, lines 7-14). Altavela is used in the outstanding Office Action to show that further polishing may not be required.

The cited reference of Arit discloses an additional ring of specially grown thermal oxide that surrounds the active area of a chip to act as a crack stopper and prevent the wafer sawing from producing chips that penetrate the active area. Arit is used in the outstanding Office Action to show that it is known in the art that wafer sawing creates cracks.

Applicant respectfully submits that Arit suggests increasing the size of the die by at least the width of the separately grown oxide ring, which is greater than 5 microns plus a safety region that is also greater than 5 microns (see figure 2 and col.3, lines 13-29), adding more than 20 microns to both the length and the width of the IC die. Applicant submits that this teaches against, or away from, the present invention having an "integrated circuit die which is slightly smaller in length and width than a conventionally produced die", and that a "size reduction of

nearly 100 μm in length and width may be quite significant in some applications" (see page 3, lines 1-2 and page 7, lines 11-12).

Applicant respectfully submits that one of ordinary skill in the art would not be motivated to combine a reference such as Arit having an additional 20 microns of die size and width, with the other suggested combinations of references, to obtain the present claimed invention that reduces the die size. Applicant submits that the suggested combination is improper as lacking motivation to combine.

Applicant respectfully submits that the suggested combination of references would not provide motivation for one of ordinary skill in the art to combine their teachings to obtain the present invention to reduce the size of the IC die. There is no suggestion in the cited references to reduce the size of the die, and at least one reference has a method that actually increases the die size by 20 microns. Thus the suggested combination is improper as lacking motivation to combine, since none of the references are addressed to, or suggest reducing the scribe line to circuitry distance.

Applicant respectfully disagrees with the suggestion on page 8 of the outstanding Office Action that the Boruta reference suggests a "... *planar perimeter side surface of the semiconductor die being a flat surface substantially perpendicular to the first planar surface* ...", as recited in claim 11, since Boruta has either stepped edges (figure 2), or beveled edges (figure 3, figure 4 and figure 5).

Applicant respectfully submits that the suggested combination of references neither describes nor suggests at least the combination of features of "... *a first planar surface having a first region with active circuitry thereon surrounded by an unused blank second region; one or more planar perimeter side... having a surface substantially perpendicular to the first planar surface ...within approximately 5 microns of an edge of the first region...*", as recited in independent claim 11, as amended herein. None of the cited references suggest a die edge close to the circuitry edge, and at least one reference teaches against this. The other independent claims are believed to be patentable for similar reasons over the suggested combination of references.

The dependent claims are believed to be in patentable condition at least as depending upon base claims shown above to be patentable over the suggested combination of references.

In view of the above discussed amendments, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney David Suhl at (508) 865-8211, or the undersigned attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Kate Gannon ______________________

Name

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